What is claimed is:

1. a channel equalizer, comprising:

an equalizer filter for correcting an error upon receipt of a signal transmitted by a sending end;

a DD slicer for calculating a first error upon receipt of the corrected signal from the equalizer filter;

a Sato slicer for calculating a second error upon receipt of the corrected signal from the equalizer filter; and

a DD error size calculation unit for taking the absolute value of the real part and imaginary part of the first error calculated from the DD slicer, summing them, and then obtaining the absolute value of the error.

2. An error control method for a channel equalizer, comprising the steps of:

multiplying a first error calculated from a DD slicer and a second error calculated from a Sato slicer each by a scale constant;

taking the absolute value of the real part and imaginary part of the first error calculated from the DD slicer, summing them, and then obtaining the absolute value of the first error;

obtaining the absolute value of an inverse response signal of a channel by multiplying the absolute value of the first error by the second error multiplied by the scale constant and adding the resultant value to a first error multiplied by the scale constant; and

generating a filter tab coefficient to reproduce a signal transmitted from a

sending end by feeding back the absolute value of the inverse response of the channel signal to the equalizer filter.

3. The method according to claim 2, wherein the equation for obtaining the inverse response of the channel and the equation for taking the absolute value of the real part and imaginary part of the first error will be expressed by:

$$e_k^G = k_1 e_k + k_2 |e_k| e_k^S$$

$$|e_k| = |e_I| + |e_Q|$$

where e_k^G is a G-pseudo error representing the inverse response of the channel of the current time, e_k is a first error calculated from the DD slicer of the current time, e_K^S is a second error calculated from the Sato slicer of the current time, e_I is the real part of the first error calculated from the DD slicer, and e_Q is the imaginary part of the first error calculated from the DD slicer; and

where the number of gates is reduced and operating time or complexity is improved by taking the absolute value of the real part and imaginary part of the first error and adding them.

4. The method according to claim 2, wherein the size of the first error and the size of the second error are adjusted to a similar size by setting the size of the scale constant by which the first error calculated from the DD slicer is multiplied 3-4 times larger than the size of the scale constant by which the second error calculated from the Sato slicer is multiplied.